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2005 J. Phys.: Condens. Matter 17 V1

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VIEWPOINT

Atomically controlled interfaces for future nanoelectronics

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Received 19 April 2005

Published 13 May 2005

Online at stacks.iop.org/JPhysCM/17/V1

Device miniaturization, speed of operation, and lower power demands are all responses to consumer needs. These driving forces are at the origin of the spectacular development of the microelectronic Si-based technology, characterized by an exponential scaling behaviour which has been persisting for over four decades [1].

During this extended period of time, this technology has almost exclusively relied on the extremely convenient physical properties of the Si–SiO₂ interface, the interface between crystalline silicon and its thermal oxide [2, 3]. In the present generation, gate-oxide layers are grown with thicknesses around 20 Å and with interfaces which are nearly abrupt at the atomic scale. Furthermore, specific nitrogen concentration profiles are engineered across the thin film to control the diffusion of dopants [3]. Further scaling of the Si–SiO₂ system is now prevented because of fundamental limits associated to leakage currents and reliability concerns [1]. Overcoming these limitations will require the use of alternative gate-oxide materials, of higher dielectric constant (high- κ materials) than SiO₂ [4]. The ability to control both the atomic structure and composition of these new oxide layers is emerging as one of the major challenges for the next generation of Si-based electronic devices. Controlling the atomic properties of thin dielectric films is currently becoming a relevant issue also for the development of oxide-based devices with other functional properties. Recent reports on surprising magnetic properties in oxides, including room-temperature ferromagnetism with giant magnetic moments, offer new perspectives for the development of magneto-optic and spin-electronic devices that could operate in ambient conditions [5–7]. The fundamental nature of the dielectric response in thin-film ferroelectric perovskite oxides is currently being addressed in view of identifying key materials for the development of novel random access memory technology [8]. Other relevant developments include the fabrication of field-effect transistors based on perovskite oxides as active elements [9] and atomically engineered hetero-oxide interfaces showing unusual charge states with surprisingly high carrier mobilities [10]. In all these developments, sophisticated oxide films play the central role.

The current gate dielectric in Si-based devices is far from the typical system of condensed matter physics. It is neither homogeneous nor isotropic, nor is the system in equilibrium, such that most properties can be obtained from an approximation to the state of lowest free energy. The processing and operating conditions introduce complexities, including the need to understand electronic excited states, quantum tunnelling, and the role of electron–phonon coupling near interfaces between media as different as silicon and oxides like amorphous SiO₂ or crystalline HfO₂. Their technological relevance for the microelectronic device industry has ensured that semiconductor–oxide interfaces have physically been characterized by a wide range of experimental techniques. In the case of the Si–SiO₂ interface, these include photoemission spectroscopy [11], ion-scattering [12–14], x-ray scattering [15, 16], electron-energy-loss spectroscopy [17], transmission electron microscopy [18], electron spin resonance [19], photodiffraction spectroscopy [20], optical reflectance spectroscopy [21], and nonlinear optical spectroscopy [22]. The complexity and the wealth of the underlying physical phenomena set challenges to which the best theory and modelling should provide insight and guidance. At this specific time, the reach of the atomic-scale regime on the one hand and the necessity of addressing new materials on the other hand are bringing to the forefront a variety of issues which call for a theoretical understanding. The relevance of these issues is pushing new ideas of structure and atomic and electronic processes in condensed matter physics and materials science, of which the impact might reach far beyond the research area of microelectronic devices.

In the current regime, the transition region at the interface between the semiconductor substrate and the gate oxide constitutes a significant fraction of the device calling for an atomic-scale understanding of the fundamental processes occurring at the interface. Such processes include the oxidation mechanism, the role of hydrogen, the defect generation process, the diffusion of dopants, and breakdown processes. As far as the modelling of such atomistic processes is concerned, there is still an enormous gap between the actual process going on in a processing step and the computer simulation. Dynamic simulations are rare and not always helpful, given the large spread of relevant timescales. Furthermore, the theoretical treatment generally introduces several approximations, such as short times, small model systems, neglect of strain build up, limited statistics, approximate structural models, equilibrium state, and zero temperature. Nevertheless, first-principles modelling approaches based on density functional theory have increasingly been applied to the study of such atomic processes [23–27]. However, the domain of application of such techniques remains limited unless combined with computationally less expensive methods. It is anticipated that the development of multiscale approaches spanning several time or length scales through the sequential use of increasingly simplified methodologies will be the only way to address complex atomistic processes at semiconductor–oxide interfaces [28–31]. For gate dielectrics, there has been strong progress on growth processes, yet there has been relatively limited analysis of how modelling might lead to oxide with fewer fixed charges or traps. The modelling of breakdown and routes to minimize degradation has been even more limited, with much of the work being phenomenological and statistical in nature.

A successful replacement for SiO₂ as gate oxide is subject to specific conditions of band alignment at both the interface with the gate electrode and the interface with the silicon substrate. To identify promising materials, it appears imperative to acquire a predictive theoretical tool for investigating band offsets at interfaces, including interface dipoles. As standard density functional calculations underestimate the band gap, their capability of predicting band offsets is questionable [32–34]. At this time, *GW* calculations [35] do not appear to offer a viable solution for carrying out systematic investigations, due to their excessively high computational cost. An alternative theoretical tool involving the same level of complexity as ordinary total energy calculations is therefore highly desirable. Such an approach

appears within reach since simplified models based on the alignment of charge neutrality levels offer quite successful predictions [36]. The issue of aligning energy levels correctly also emerges when defect levels need to be situated with respect to the band extrema [37, 38].

High- κ materials such as ZrO_2 and HfO_2 and their silicates are currently being considered as promising alternatives to SiO_2 [4]. As opposed to SiO_2 , these materials give rise to important concentrations of oxide defects [39–41], which contribute to degrading the electrical performance of the device. Currently, an important research effort is being devoted to the characterization of these defects. Similarly, the presence of defects of unknown origin at SiC– SiO_2 interfaces prevents the SiC-based technology from making progress [42]. Furthermore, the role that defects play in affecting properties such as the mobility [43] or the (soft) breakdown [44] represent great open issues. It is therefore clear that the identification of defects constitutes a major challenge for modelling approaches. When the defect centre is paramagnetic, electron spin resonance experiments provide indications on its atomic structure and may ultimately lead to its identification [45–47]. By contrast, diamagnetic centres offer no direct information on their origin. Traditionally, theoretical investigations focus on crystalline systems as parent structures for defect generation. Only recently disordered model structures and their full statistical variety have been considered for the study of defects [28–30, 48]. Another difficulty in modelling defect centres in amorphous environments originates from the fact that model defects are generally constructed on the basis of defect-free structures. While this appears justified for defects in crystals, this procedure applied to amorphous materials might miss relevant defect structures.

The search for alternative oxides motivates recent theoretical studies aiming at predicting the dielectric permittivity [49–52]. While ordinary density functional calculations are very successful in coping with crystalline materials, the study of amorphous systems often exceeds present computational resources and requires the development of simplified schemes [49]. Furthermore, it becomes increasingly evident that future gate stacks will be composed of several atomically thin layers with physical properties differing significantly from their bulk counterparts. The study of the permittivity of such stacks is driving new theoretical studies in which the local evolution of the permittivity is addressed [53, 54].

The understanding of transport properties is another theme of paramount importance. The way the inhomogeneities [43] and soft phonons in the oxide [55] affect the mobility clearly has direct implications on the electrical quality of the device. At present, the modelling of transport properties in nanoelectronic systems is a growing research area in the theoretical community [56–58]. One might expect that new developments will find early application in the Si-based research area, given the prominent role of electrical measurements in this field.

As required functions of future nanoelectronic devices will diversify, different demands will need to be satisfied, leading to radical materials challenges at least for some functions. Foreseeable devices integrated in standard Si-based chips include high-speed optical modulators [59, 60] and quantum gates for high-temperature operation [61]. Future electronics might even involve materials other than silicon. For instance, carbon-based materials are under scrutiny for some functions [62], and germanium-based devices with high- κ gate oxides have been identified as alternatives to meet the severe scaling requirements of the next generations [63, 64]. In perspective, as developments in nanoelectronics address an increasing range of functions and materials, great opportunities lie ahead for theory and modelling to play a leading role.

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